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| PTO-1449 (Modified)<br>U.S. DEPARTMENT OF COMMERCE<br>PATENT AND TRADEMARK OFFICE<br>INFORMATION DISCLOSURE STATEMENT BY APPLICANT | ATTY. DOCKET NO.<br>RMBS.002 | SERIAL NUMBER<br>09/303,609 |
|---|---|---|
| | APPLICANT<br>S. SIDIROPOULOS | |
| | FILING DATE<br>MAY 3, 1999 | GROUP ART UNIT<br>2734 |

**U.S. PATENT DOCUMENTS**

| EXAMINER INITIALS | DOCUMENT NUMBER | DATE | NAME | CLASS | SUB CLASS | FILING DATE |
|---|---|---|---|---|---|---|
| cf | 5,727,037 | 03/10/98 | Maneatis | 327 | 158 | |
| cf | 5,614,855 | 03/25/97 | Lee et al | 395 | 396 | |
| cf | 5,796,673 | 08/18/98 | Foss et el. | 365 | 233 | |

**FOREIGN PATENT DOCUMENTS**

| EXAMINER INITIAL | DOCUMENT NUMBER | DATE | COUNTRY | CLASS | SUB CLASS | TRANSLATION YES/NO | |
|---|---|---|---|---|---|---|---|
| | | | | | | | |

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| cf | J. Maneatis, "Low-jitter process-independent DLL and PLL based on self-biased techniques," IEEE Journal of Solid-State Circuits, vol, 31, no. 11, pp. 1723-1732, (Nov. 1996) |
| cf | S. Sidiropoulos et al. " A Semi-digital dual Delay Locked Loop", IEEE Journal of Solid-State Circuits, vol, 32, no. 11, pp. 1683-1692, (Nov. 1997) |
| cf | B. Garlepp et al., "A Portable Digital DLL Architecture for CMOS Interface Circuits", Proceedings of the 1998 Symposium on VLSI Circuits, pp. 214-215, (June 1998) |
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| EXAMINER Chih Min Tan | DATE CONSIDERED 4/11/02 |
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EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.

#3



| PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE | ATTY. DOCKET NO. RMBS.002 | SERIAL NUMBER 09/303,669 |
|---|---|---|
| | APPLICANT S. SIDIROPOULOS | |
| INFORMATION DISCLOSURE STATEMENT BY APPLICANT | FILING DATE MAY 3, 1999 | GROUP ART UNIT 2734 |

**U.S. PATENT DOCUMENTS**

| EXAMINER INITIALS | DOCUMENT NUMBER | DATE | NAME | CLASS | SUB CLASS | FILING DATE |
|---|---|---|---|---|---|---|
| cf | 5,412,349 | 05/02/95 | Young et al. | 331 | 34 | |
| cf | 5,334,953 | 08/02/94 | Mijuskovic | 331 | 8 | |
| cf | 5,477,193 | 12/19/95 | Burchfield | 331 | 8 | |
| cf | 5,687,201 | 11/11/97 | McClellan | 375 | 376 | |
| cf | 5,126,692 | 06/30/92 | Shearer et al. | 331 | 8 | |
| cf | 5,166,641 | 11/24/92 | Davis et al. | 331 | 1A | |
| cf | 5,334,951 | 08/02/94 | Hogeboom | 331 | 1A | |
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| cf | F. M. Gardner, "Charge-Pump Phase-Lock Loops", IEEE Trans. Comm., vol. COM-28, pp. 77-86, (Nov. 1980) |
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| cf | D. Mijuskovic et al., "Cell-Based Fully Integrated CMOS Frequency Synthesizers", IEEE Journal of Solid-State Circuits, vol 29, no. 3, pp. 271-279, (March 1994) |
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| cf | K. Lee et al., "A CMOS Serial Link for Fully Duplexed Data Communication", IEEE Journal of Solid-State Circuits, vol 30, no. 4, pp. 353-363, (April 1995) |
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| EXAMINER Chuck Mi Fan | DATE CONSIDERED 4/11/02 |
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